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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/985,768	11/06/2001	Kwame Osei Boateng	826.1767	4333
21171	7590	12/13/2005	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			SIEK, VUTHE	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/985,768	BOATENG, KWAME OSEI	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/10/05</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to application 09/985,768 and amendment filed on 9/20/2005. Claims 1-13 remain pending in the application.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 and 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kajihara et al., "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504.

4. As to claims 1 and 10-13, Kajihara et al. teach new cost-effective heuristics for a generation of minimal test sets (compacted set of test stimuli) for a digital circuit (see whole article) comprising fault simulation under double detection (starting page 1498, section D.); selecting essential test stimuli from among subsets of the set of test stimuli after mapping between the test stimuli and the faults has been established by the simulation, where an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of the test stimuli (page 1500, section III. A STATIC COMPACTION TECHNIQUE, especially section A. describes mapping between test stimuli and faults for example consider five faults: {f1, f2, f3, f4, f5}; suppose that three test vectors t1, t2 and t3 are generated; let  $\det(t1) = \{f1, f2, f3\}$ ;  $\det(t2) = \{f3, f4\}$ ; and  $\det(t3) = \{f5\}$ ; an eliminating redundant test

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stimuli form among subsets of test stimuli after selecting the essential test stimuli from each subset (page 1500, section III. A STATIC COMPACTION TECHNIQUE, especially section B., describing how to remove or eliminating redundant test stimuli in order to form a smaller subset of test stimuli; section A describes test vectors t2 and t3 are removed from the test set making test set become smaller); and an output device outputting a compacted set comprising the selected essential test stimuli (see at least section III. A STATIC COMPACTION TECHNIQUE starting page 1500, especially Table IV shows an output result). The redundant test stimulus is a test stimulus that detects a fault, which is detectable by another test stimulus in each subset after the selection of the essential test stimuli (section 2. page 1499, see Table IV).

5. As to claims 2-5 and 7-9, Kajihara et al., teach outputting a minimum-sized subset of the set of test stimuli, which covers faults without modifying test stimuli in the minimum-sized subset, as the compacted set; hierarchically repeating selecting of essential test stimuli after eliminating of redundant test stimuli to output the compacted set comprising the selected essential test stimuli; identifying a subset of test stimuli that optimally covers a given set of faults and eliminating one or more test stimuli other than the identified test stimuli as the redundant test stimuli; storing information of faults which the set of test stimuli cover, and pointing information associating each test stimulus with the faults detectable by a corresponding test stimulus; the faults including a stuck-at fault and a delay fault; performing compaction of the set of test stimuli by regarding a sequence of initializing, sensitizing, and propagation subsequences as a single test stimulus (See at least Section III, Table IV).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Kajihara et al., "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504.

8. As to claim 6, Kajihara et al. teach using a fault simulation to search and detect essential faults of a test in the test set. As shown in Table IV, number of test of the test set, number of faults and number of check are described. It is well known to practitioners in the art that a counter is used to store information related application in order to facilitate a process of increasing or decreasing an information number stored in the counter. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to have stored counter information as recited in the claim in order to facilitate the fault simulation to obtain information as shown in Table IV as expected, thereby a compacted set comprising of essential test stimuli is finally obtained.

***Remarks***

9. Examiner has maintained the rejection under Kajihara. Applicant argued that Kajihara is not particularly relevant to the present invention. It is not true. Examiner respectfully submits that Kajihara teaches each element of the claimed limitations as

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described in the above rejection because Kajihara teaches simulating, mapping stimuli and faults, selecting essential stimuli and eliminating redundant stimuli. Kajihara teaches in section A., page 1500, where the test vectors t2 and t3 can be removed because these test vectors are redundant test vectors. The test set is now become smaller {t1, t4} than {t1, t2, t3}.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



**VUTHE SIEK**  
PRIMARY EXAMINER